

Future Directions in Reconfigurable Computing

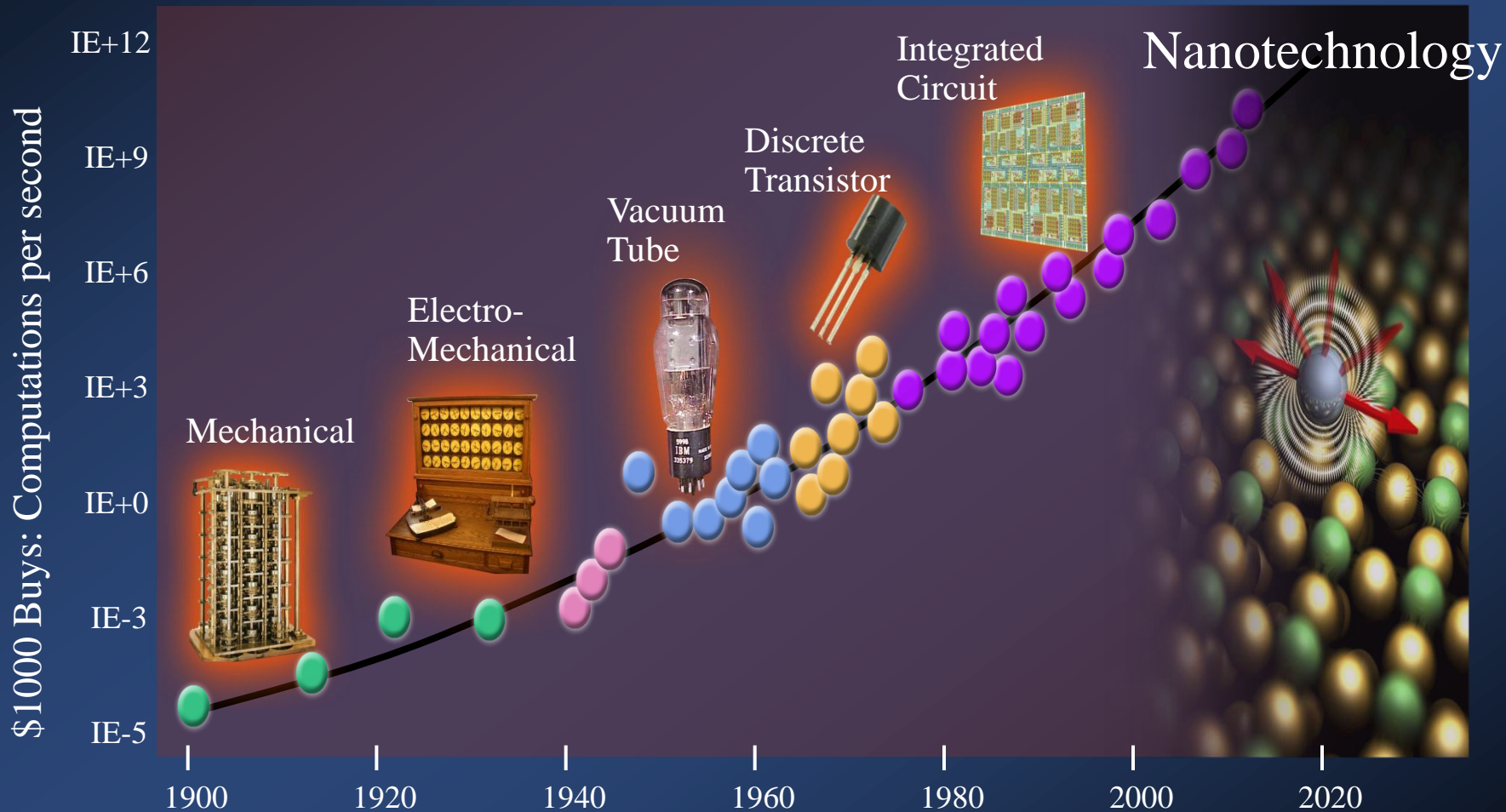
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Outline

- Brief History of Electronics
- Forward Looking Strategic Drivers
- Current Situation in Reconfigurable Computing
- Opportunities to Innovate
- Conclusions

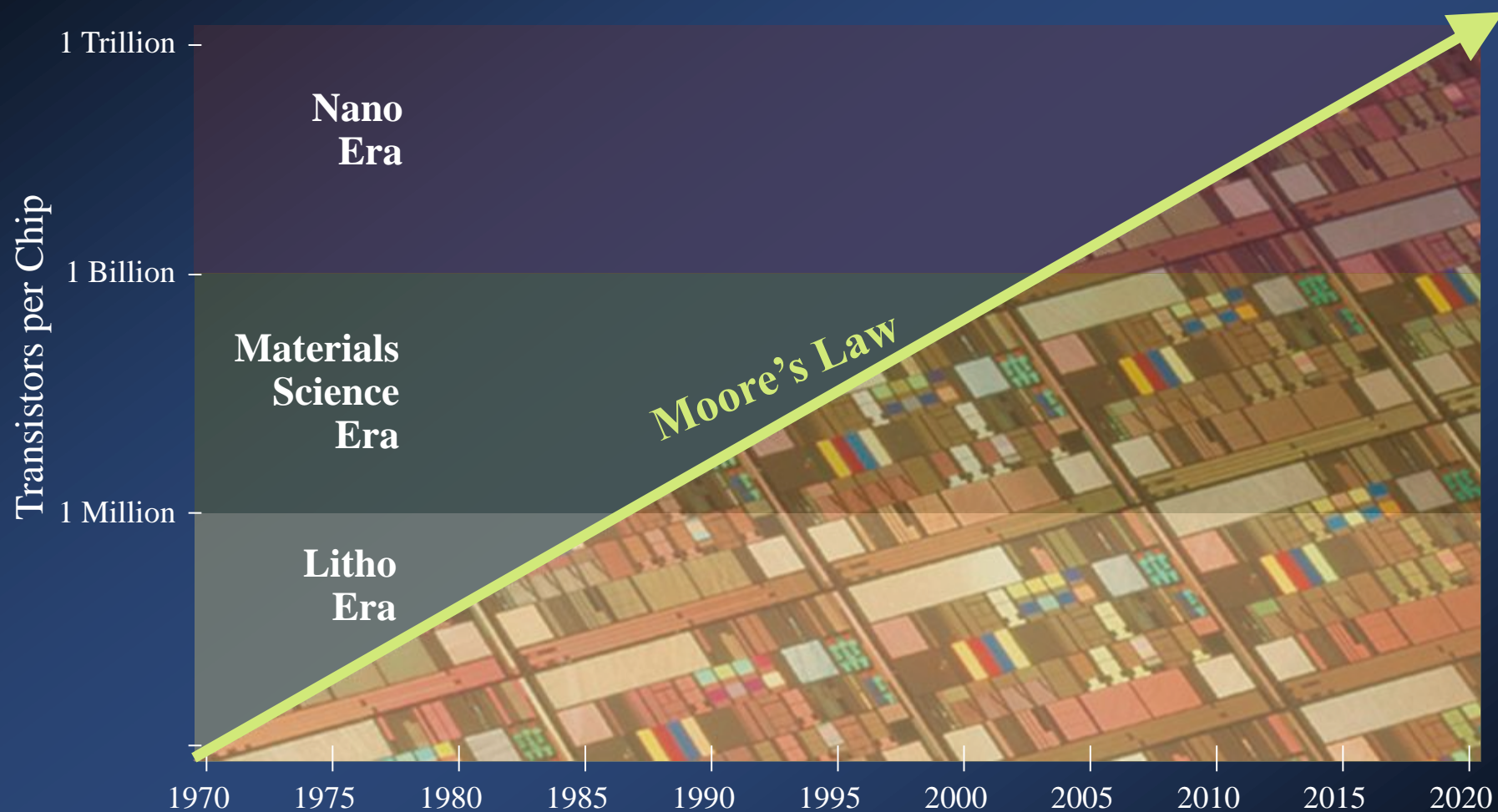
Accelerating Advances in Technology



Source: Kurzweil 1999 – Moravec 1998

Raztech LLC

Trends in Increasing Transistor Density



Architectural Progression (Technology)

- Key Abstraction Innovations:
 - ISA, VM, Shared Memory
 - HLL Languages, operating systems
- Mainline Innovations:
 - Latency Techniques:
 - Caching (istream, dstream), Prediction (istream mostly), Speculation
 - Bandwidth Techniques:
 - Pipelining, Wide Busses, Multi-processor/Multi-core
 - Smarter Compilers
 - RISC vs CISC, Performance Feedback

Architectural Progression (Technology)

- Beyond Conventional CPUs:
 - Graphics, Network, Search?
 - Range of communication for multi-core/multi-processor (Ambric to Tiler)
 - RISC vs CISC of today.
- Other Models: VLIW, Multithreaded, SIMD
- Alternative Proposed Models:
 - Reconfigurable Computing Platforms
 - Nibble-mode processors

Business Overview:

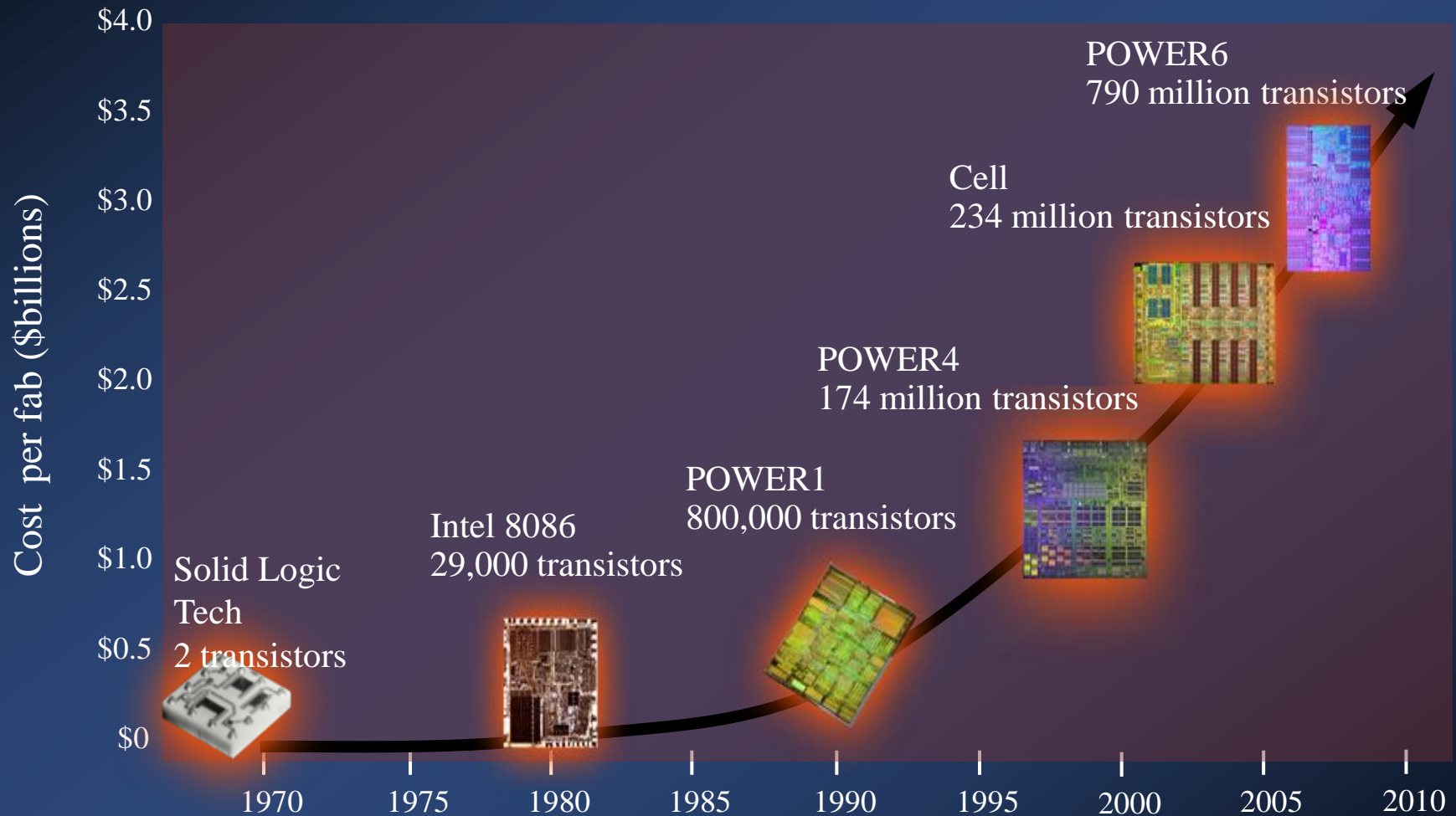
- Electronics: \$1T in the context of \$12T U.S. Economy (\$60T+ WW)
 - Semiconductors: \$200B
 - FPGA: \$3.5B
 - EDA: \$4B, PLM: \$16B

- Three Large Vertical Mega-Markets:
 - Information Technology: Computers, Laptops
 - Internet Infrastructure: Routers
 - Portable Consumer Device: cell phone, ipod
 - All else in noise:
 - Industrial, Medical, Defense, etc..

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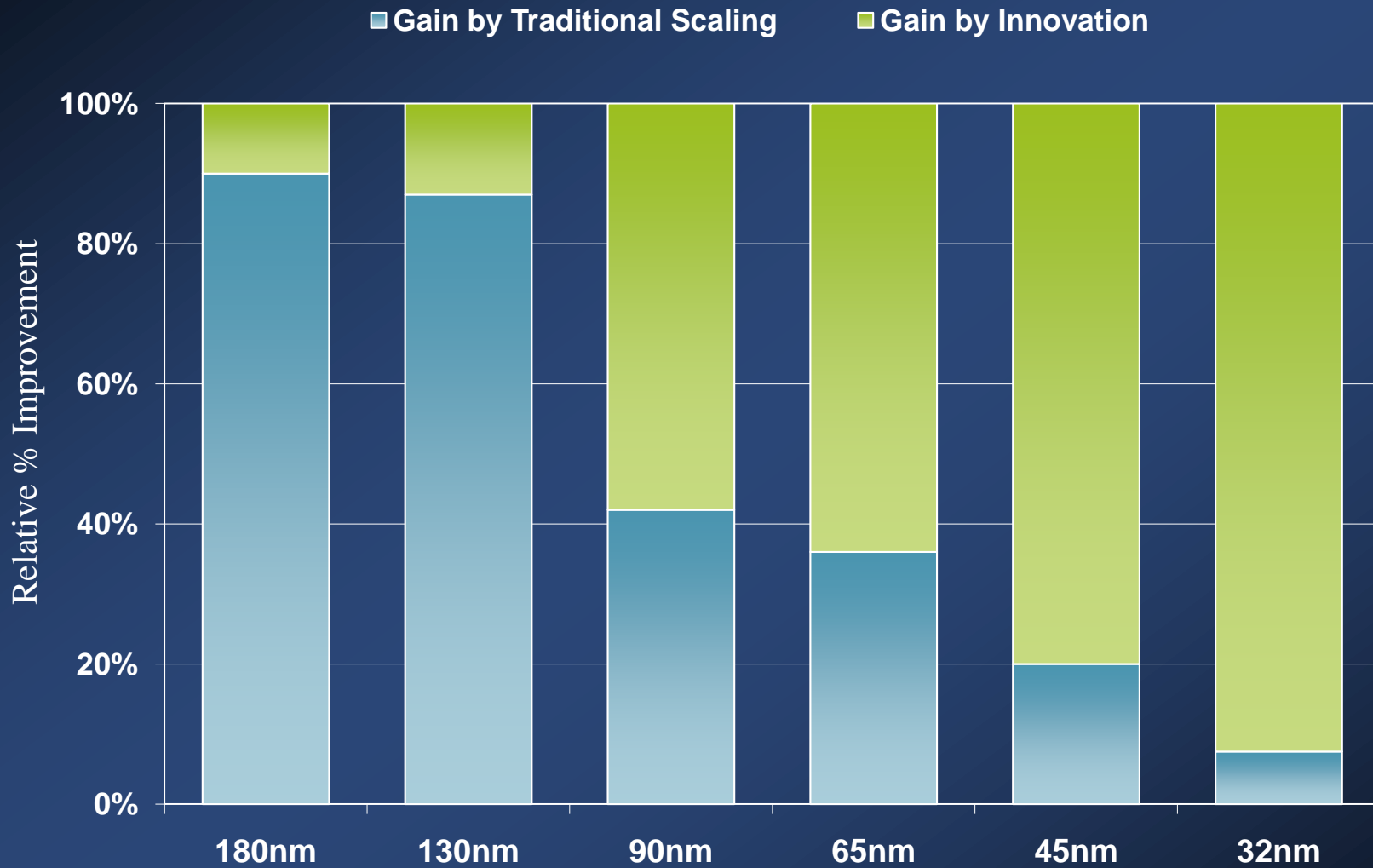
- Brief History of Computer Architectures
 - Technology and Business View
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Increasing Cost (Technology)

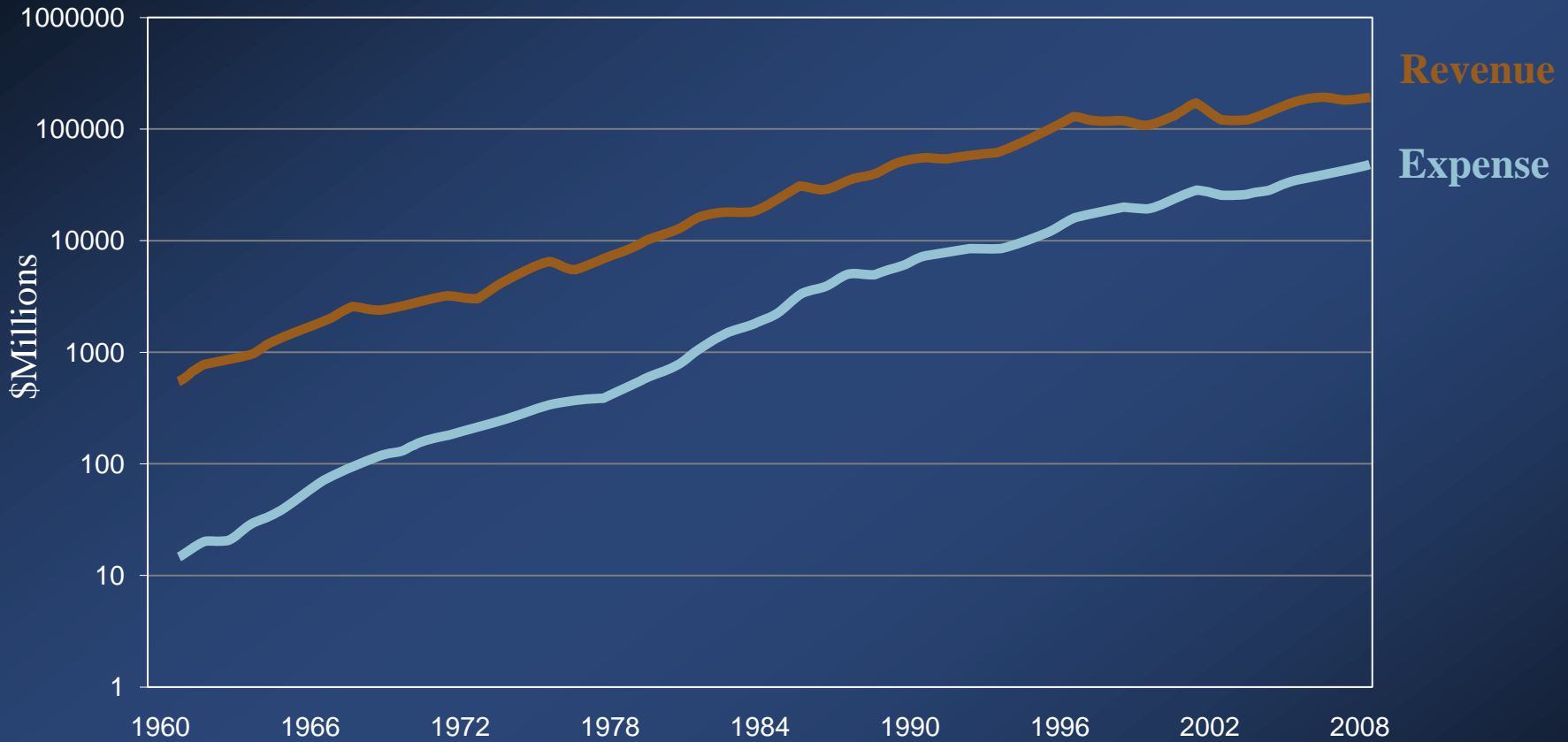


Sources: IC Insights; Intel - Historical Wafer Size Trend

IBM Transistor Performance Improvement



Semiconductor R&D Expense/Revenue

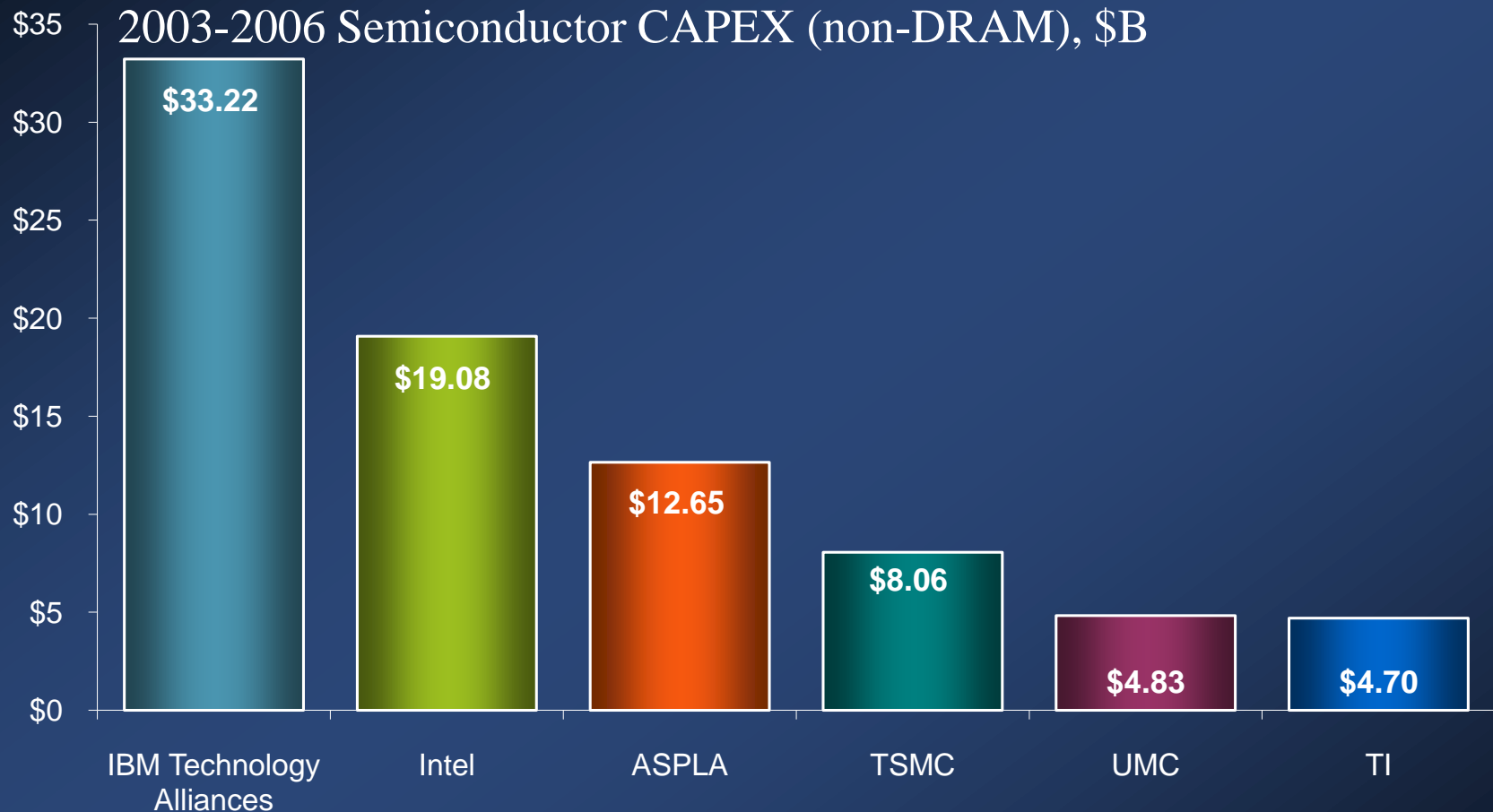


2004-20 annual revenue growth @ 6.5%, while R&D expense growth @ 12.2%

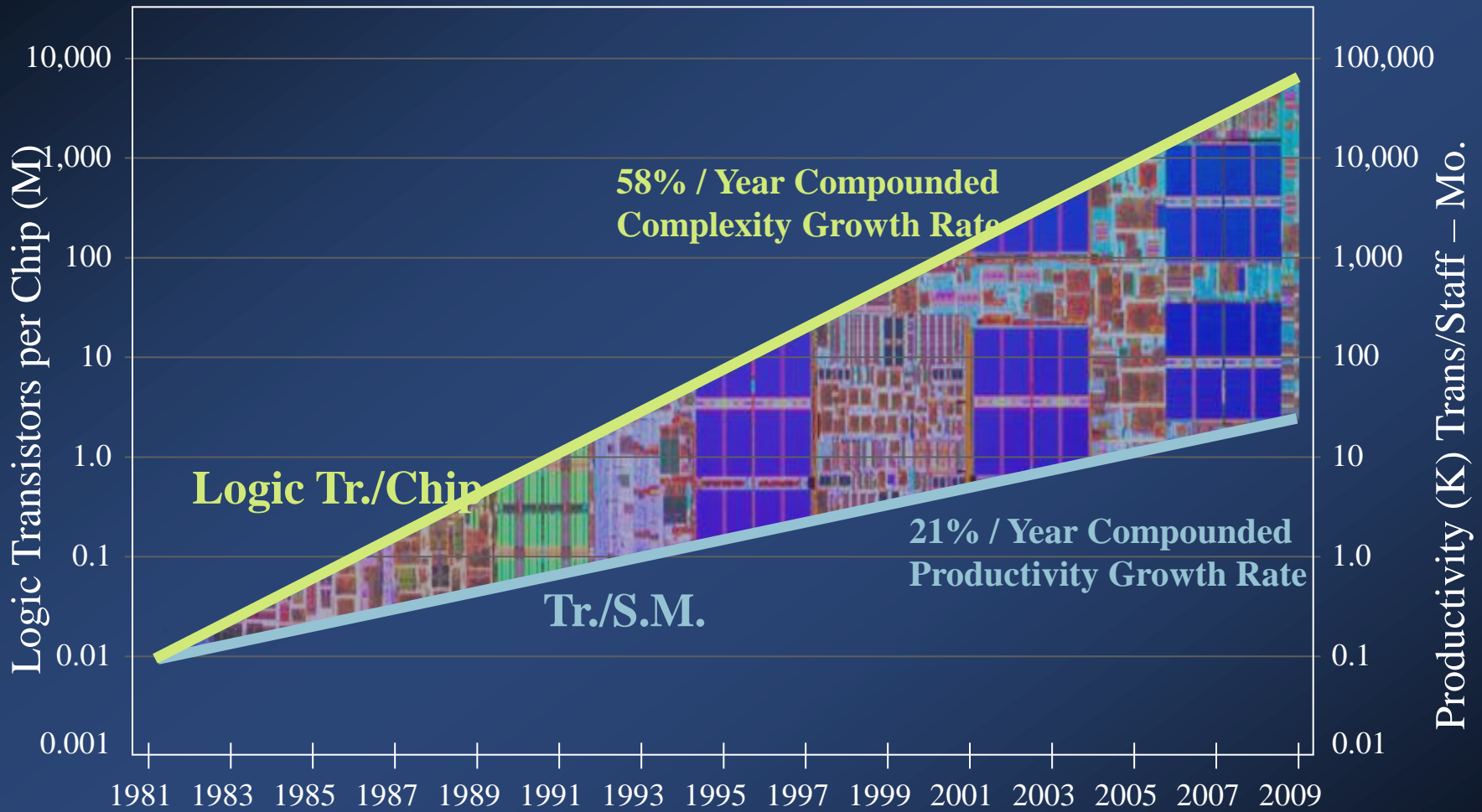
Foundry industry evolution

- Late 80s. Pure play foundry established to meet the need of manufacturing outsourcing from IDM
- Mid. 90s. Fabless boomed with COT model, alternative of ASIC
- Late 90s and early 00s. Fast growth of fabless attracted new foundries,
 - New pure play, Tower, Silterra, 1st Silicon, GSMC, SMIC
 - IDM turned foundries, Jazz, ASMC, HHNEC, Dongbu, VIS, Polar fab, Zfoundry
 - IDM offered foundry service, IBM, MagnaChip, Austriamicrosystems, Cypress
 - JV Fab with Fabless and Fab-lite, Chartered SMP, UMCi, Wafertech
- Mid 00', reality called, few foundries makes money
 - Differentiation -> Collaboration -> Consolidation started
 - Mega fab trend started
 - Samsung, Fujitsu, Toshiba in foundry game

Strategic Development Alliances: CAPEX Landscape



Design Productivity Gap



Impact on Design (Investment View)

- Cost of IC design rising rapidly and very risky
 - \$50M for 90nm
 - 2-3 years before first revenue
 - 7 years before exit event
- Applicability to volume driven markets critical
 - single large focused market or
 - Collection of markets served with single solution
- Increased focus on platforms for all vertical markets

What does this mean for computer architects ?

- A small number of very large chips in traditional markets
 - Architectural innovation providing diminishing returns
 - Growth driven by GDP
- Smaller Markets maybe big enough more platforms:
 - Bioinformatics, Cryptography, Oil Exploration, Search
 - Bets being made today: sicortex, pa-semi, pico-chip
- Environment favors small number of flexible platforms

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- **Current Situation Reconfigurable Computing:**
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Reconfigurable Computing: Core Play Today

- Assume a flexible implementation fabric (FPGA)
- Operating principles:
 - Leverage flexibility for in-context optimization (performance/power)
 - Match data type and parallelism between implementation and application
 - Leverage space vs time
- Various Levels of granularity:
 - ILP
 - Co-processor
 - System
- Two Basic Use-Models: Embedded or HPC

Reconfigurable Computing: High Level Thrusts

- ILP:
 - Research: PRISC, Chimeara, Garp
 - Commercial: ST (2007/2008)

- Co-Processor:
 - Research: Splash
 - Commercial: Nallatech, Cray, HP

- System:
 - Research: PAM, BEE2, Splash
 - Commercial: Emulation

Reconfigurable Computing: Observations:

- HPC:
 - Many studies on “unit” level performance/power advantage
 - Limited Success at the Application Level
 - Limited Commercial Success

- Embedded: some success with real-time data-flow applications
 - Radar Signal Processing
 - Image Processing

- System: some success with dedicated system solutions (logic emulation)

Reconfigurable Computing: Logic Emulation

- Two Basic Use Models:
 - Simulation Acceleration
 - In-Circuit Test
- Historical:
 - Early Systems Built with FPGA Technology (\$200M/year)
 - Issues With FPGA solution:
 - Multi-FPGA Mapping (Rent's Rule)
 - Compile-Time limiting factor for design productivity
 - Today: nibble-mode upprocessors own largest marketshare

Reconfigurable Computing: Current Status

- Limited Success: reasons cited
 - Design Flow is limited
 - FPGA support for runtime reconfiguration poor
 - Application entry point difficult
- Observations:
 - Many Issues similar to parallel uprocessor development.
 - Caught between processor and ASIC

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Reconfigurable Computing: Potential Direction

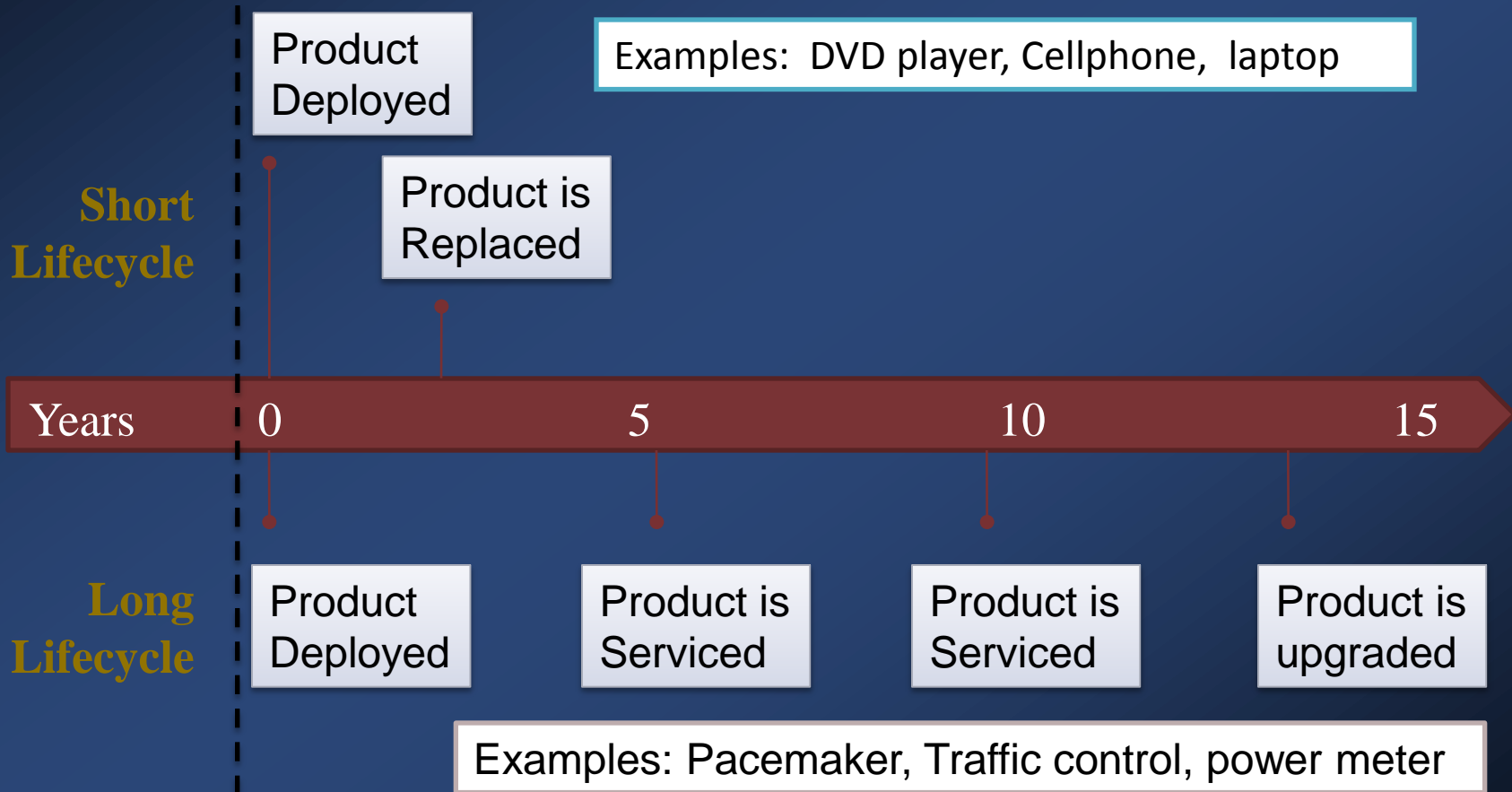
- Shift the value statement:
 - Focus on flexibility as a basic value (vs power/perf)
 - Find markets where it is inherently valued and build solutions

- Long Life Cycle Markets(LLC):
 - Cost of deployment and maintenance overwhelm initial costs
 - Which markets exhibit these characteristics ?
 - Energy, Health Care, Aerospace and Defense

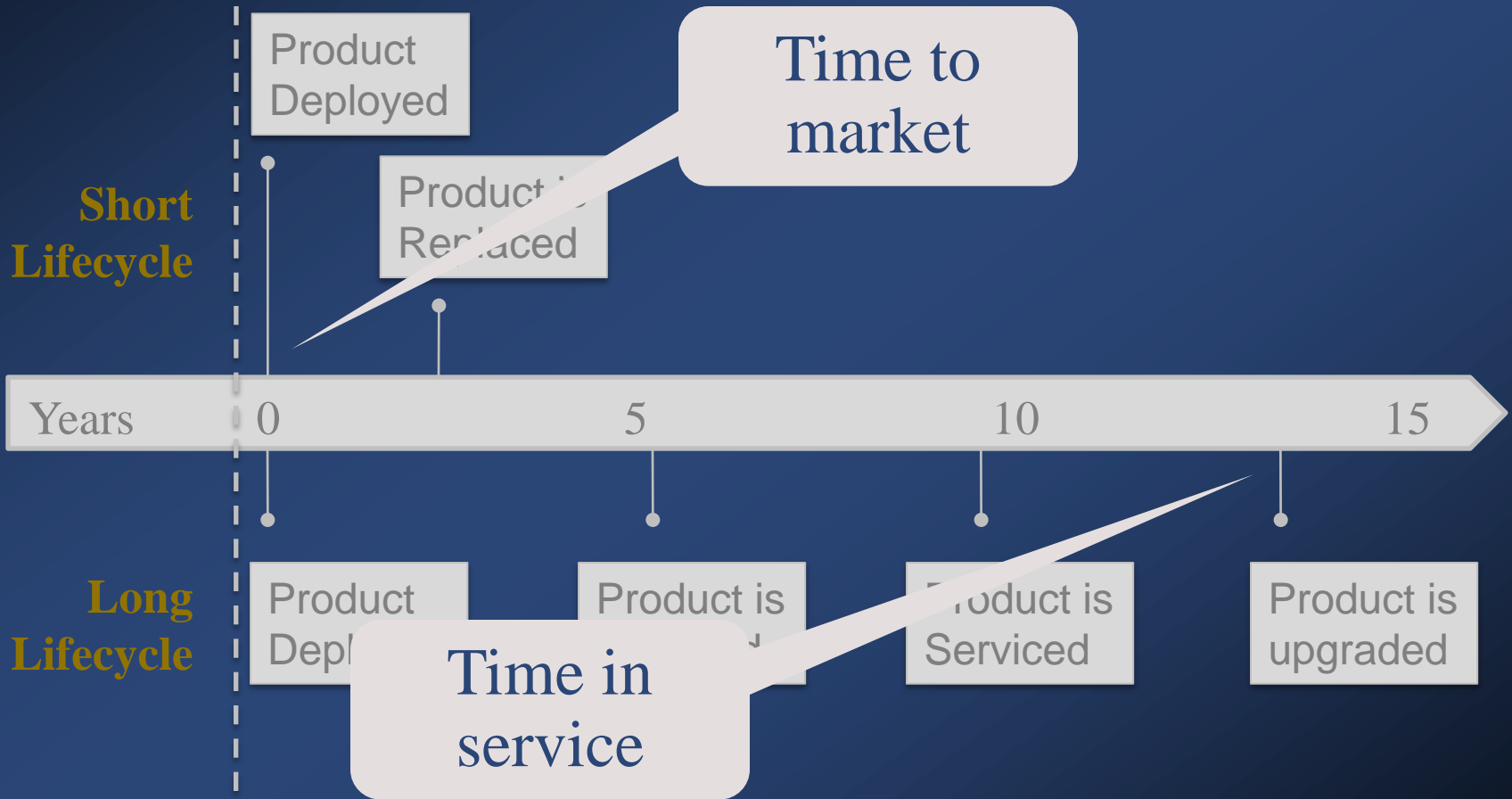
Opportunities to Innovate: LLC Products Details

- Old Mega-Markets: Product Life (< 3 years)
- New Potential Mega-Markets: Product Life (>10 years)
- New Issues:
 - Future Requirements Volatility
 - Enhanced Reliability
 - Supply Chain Integrity

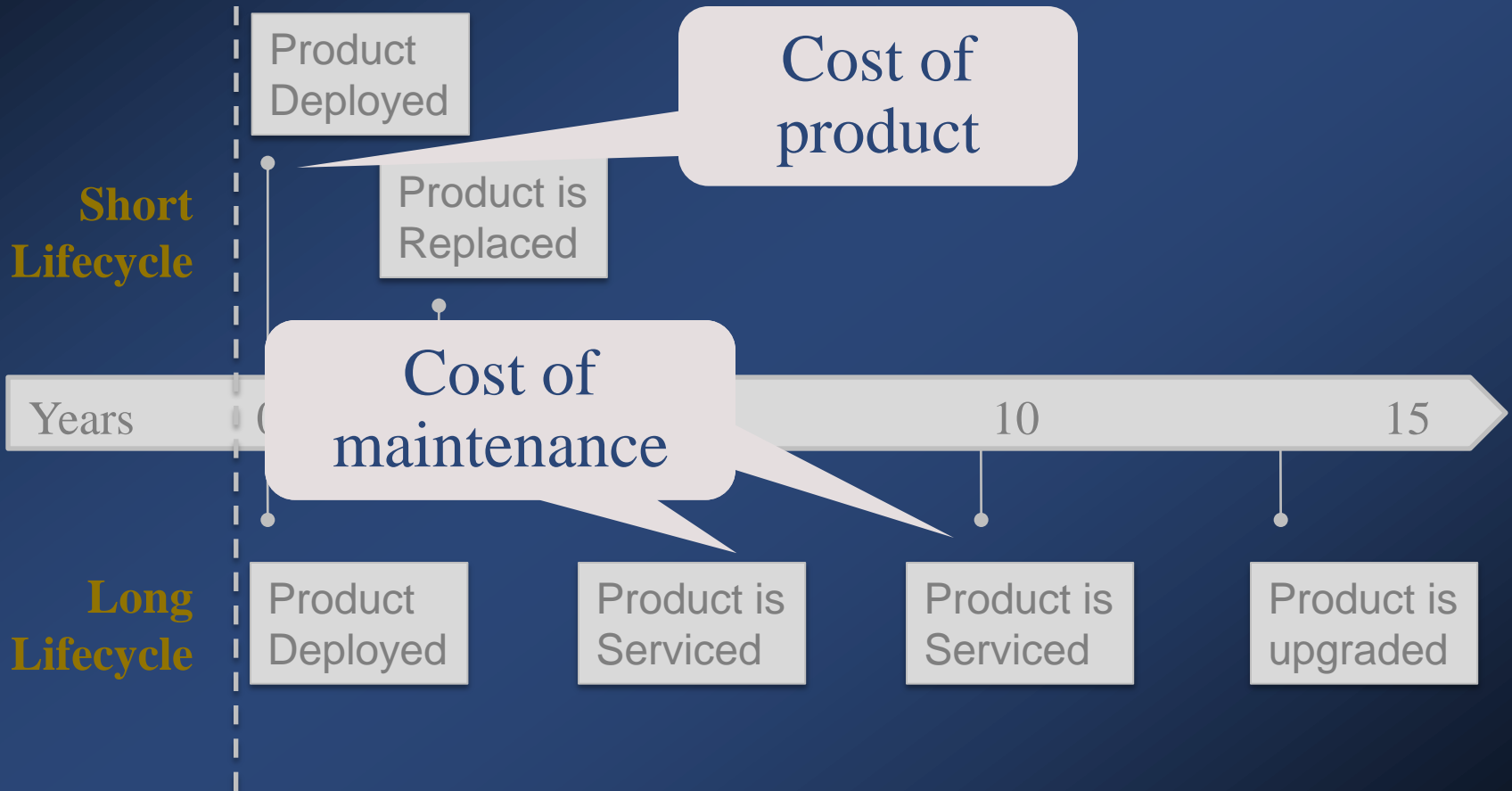
Short vs. Long Lifecycle



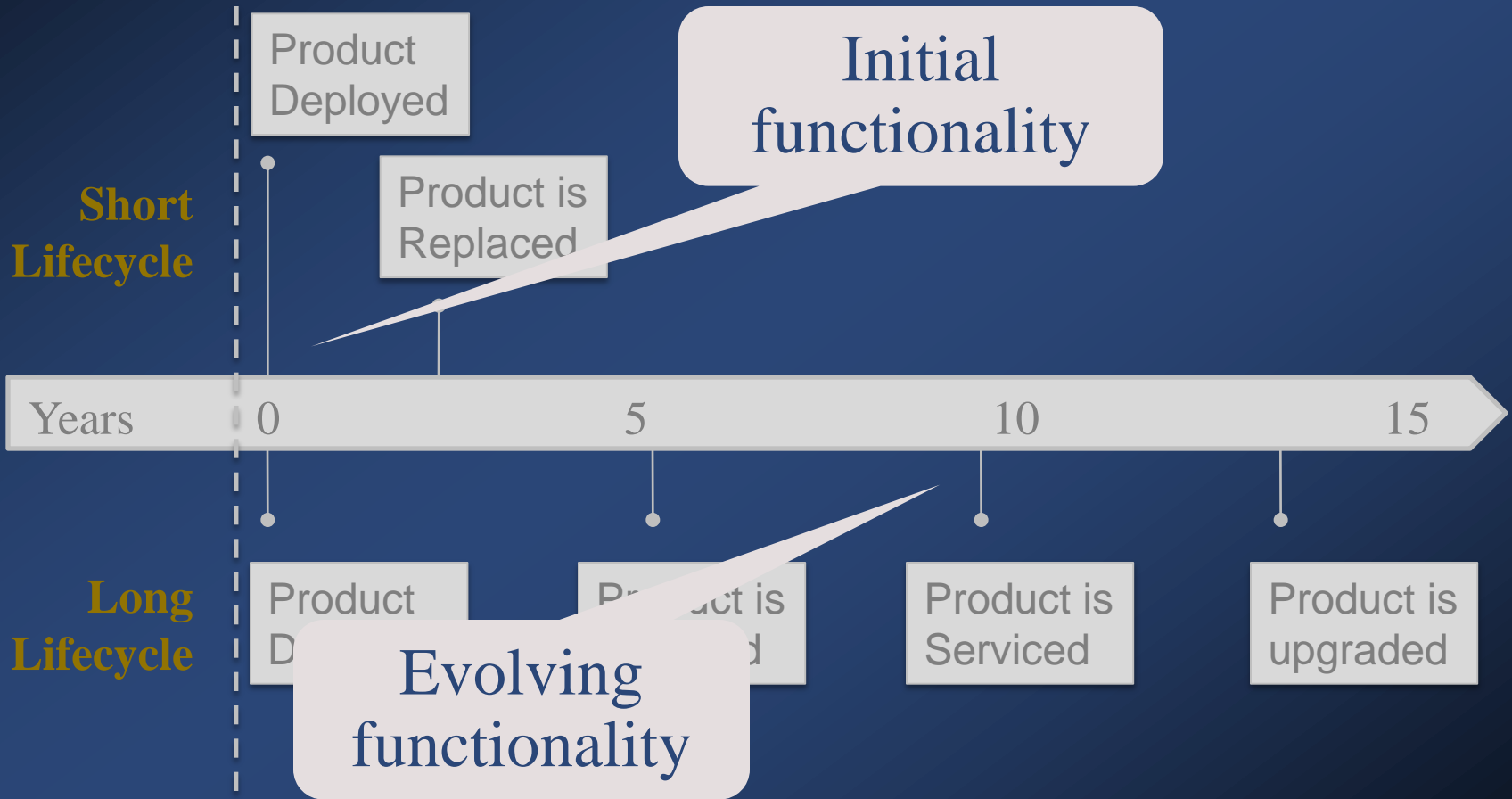
Short vs. Long Lifecycle



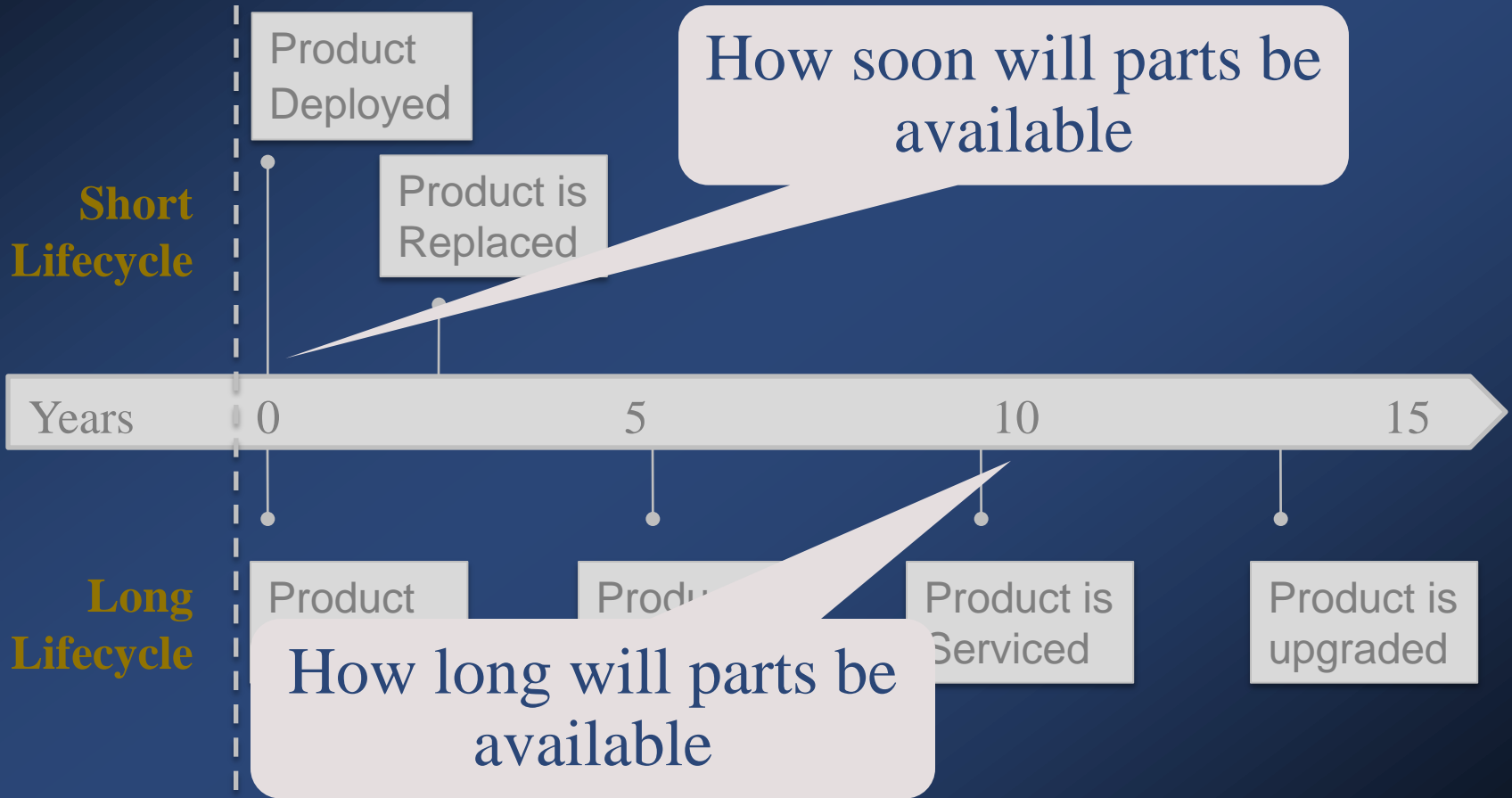
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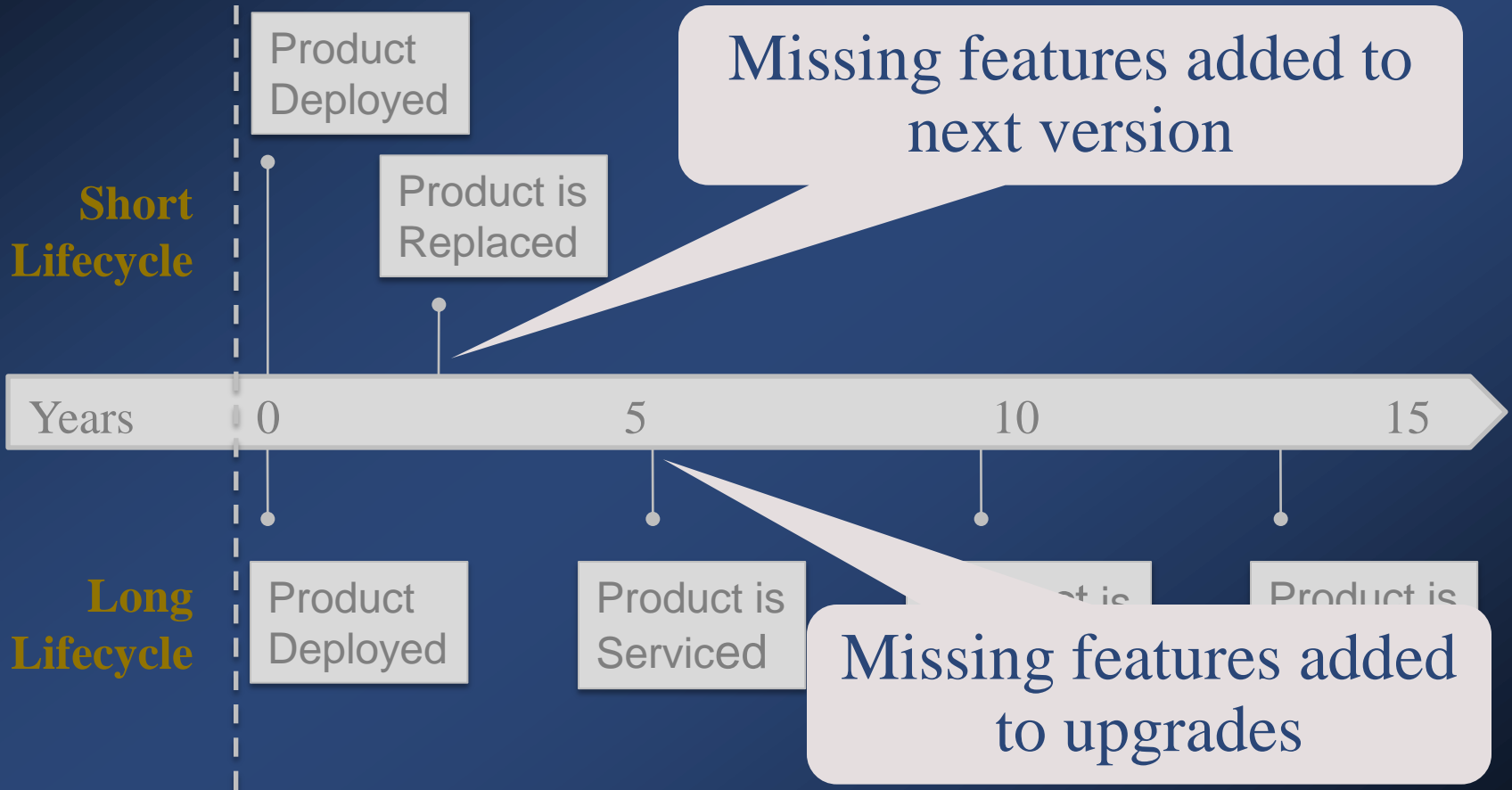
Short vs. Long Lifecycle



Short vs. Long Lifecycle



Short vs. Long Lifecycle



Long Lifecycle Solution: Programmable Fabric

- Programmable Reconfigurable fabric can resolve the major LLC issues
 - Reliability
 - Evolvability
 - Supply Chain

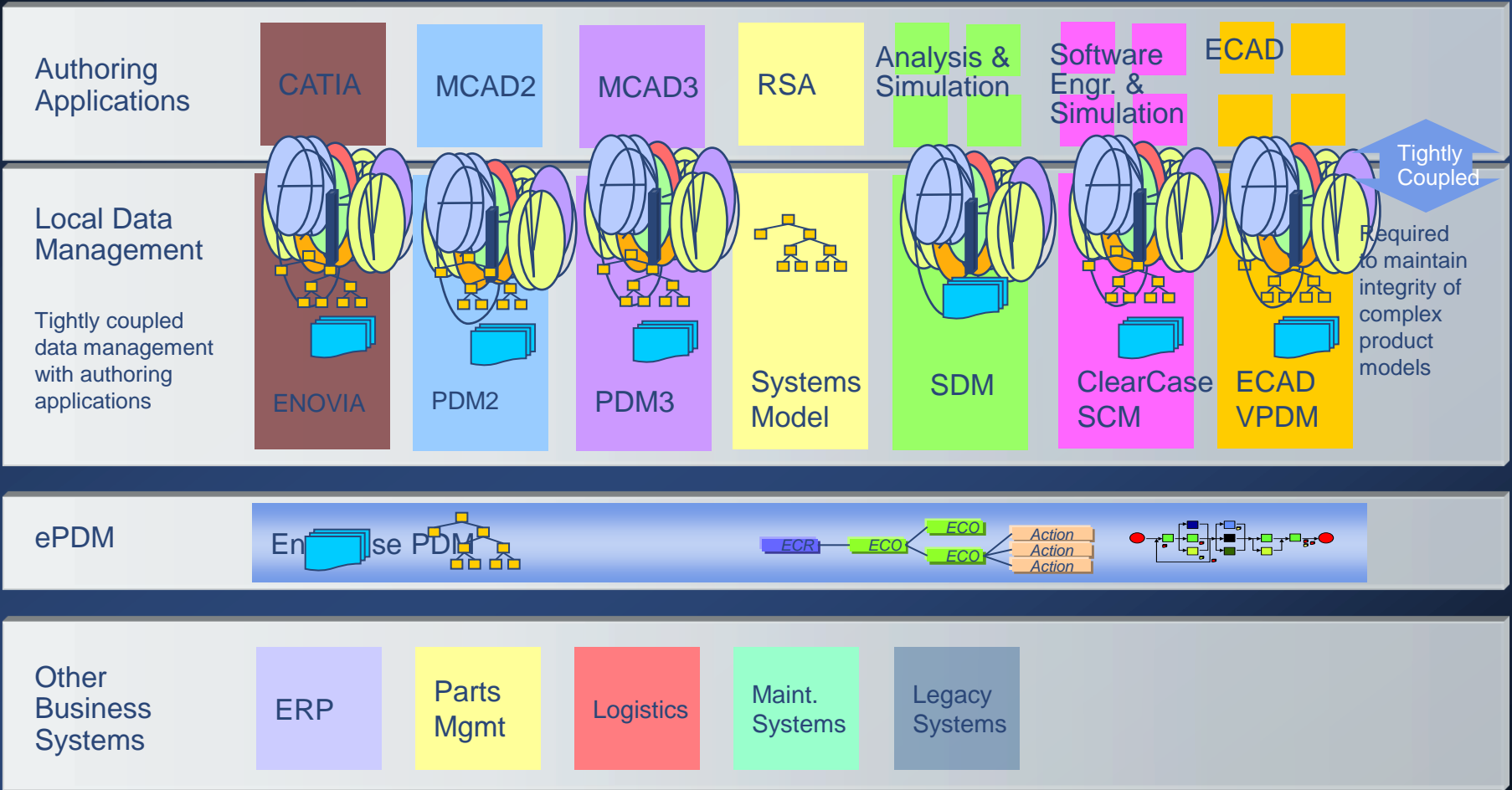
- All the years of research work on power/performance is “upside”

- Potentially rich new area, but significant challenges exist.

Long Lifecycle Solution: Research Issues

- LLC Design System:
 - What are the right metrics to capture the newer issues within the design environment ?
 - How are these metrics generated and maintained over time ?
 - Can we enhance optimization (synthesis) to account for the new metrics ?
 - How do we connect these metrics and view of lifetime cost to existing systems in the product lifecycle management space ?
- LLC Programmable Platform:
 - How do we handle uprocessors, FPGAs, and analog ?

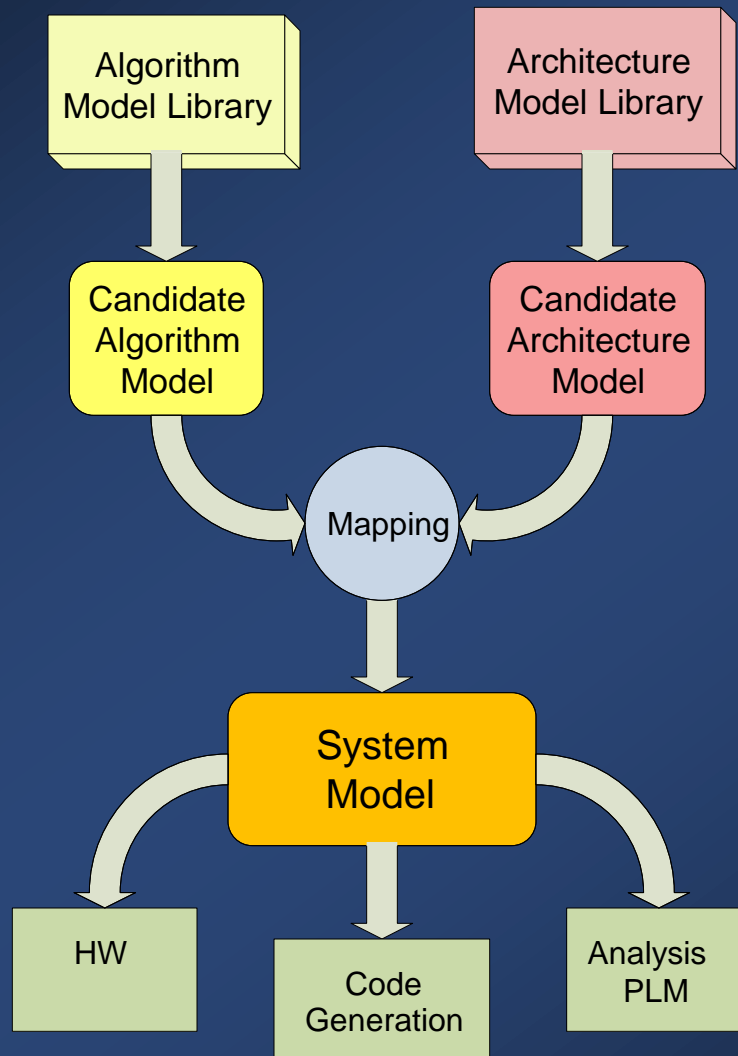
The Challenge : Traditional PLM Environment



Long Lifecycle Solution: Early Work

- LLC Design System:
 - Early Research at University of Florida
 - Spun-out into startup: www.systemcenteringsolutions.com
- Basic Idea:
 - Intercept the Design Process at the System Level (Systemc, Matlab)
 - Introduce the notion of architecture and a mapping from functional definition.
 - Generate evolvability via process of sensitivity analysis of functional definition.
 - Generate reliability and supply chain from sensitivity analysis of architecture
 - Build a total cost function from the combination of above
 - 4x-7x cost optimization shown in early prototypes

Long Lifecycle Solution: Early Work



Conclusions:

- Semi-Conductor Trends Point towards consolidation
 - Fabs and Designs
- Reconfigurable Computing has had difficulty with performance/power
 - Design Eco-System
 - Caught between uprocessor and ASIC
- Long Lifecycle Products offer an intriguing opportunity:
 - Flexibility itself is valued and can provide benefit
 - LLC Products may represent the next large markets (Energy/Medical)
- Reconfigurable computing research maybe extendable in the LLC direction.